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Description

The invention relates to means and methods for allocating resources in an electronic digital data processing system.

As is well known, an important function performed within a data processing system having mult-programming and/or multiprocessing capabilities is the allocation of the available resources to the various data processing operations being performed. The manner and efficiency of this allocation of resources can have a significant impact on system performance and economy.

Summary of the present invention

A primary object of the present invention as claimed in claim 1 is to provide particularly useful and advantageous apparatus for allocating resources in a data processing system.

The principles of the invention are applied to the function of allocating registers required for use by a plurality of tasks being concurrently performed by a data processing system. Typically, the system provides a predetermined number of registers which are allocatable for use by a plurality of active tasks. An updatable list of free and assigned registers is maintained and, as each task is activated, specially provided register selection apparatus responsive to this list selects a predetermined number of free registers for assignment to the task. If insufficient free registers are available for use by a newly activated task, it is signalled to remain in a "hold" state.

The register selection apparatus includes a plurality of specially mapped memories to which respective portions of the updatable list of free and assigned registers are applied as memory addresses for reading out selected memory words. These selected memory words identify available free registers and also provide appropriate logic for controlling a plurality of multiplexers to which the selected memory words are applied. These multiplexers operate to select a particular plurality of the available free registers for assignment to each newly activated task where sufficient free registers are available to meet the task's requirements. The sufficiency of free registers for a newly activated task is determined by comparing the number of free registers required by a task with the total number of free registers which the selected memory words indicate are available. If insufficient free registers are available for assignment to a task, the comparator provide a "hold" signal for use in placing the task in a"hold" state.

The combination of the list of free and unassigned registers, the specially mapped memories and the multiplexers, as briefly described above, provide for register allocation in a highly advantageous and economical manner which is well suited for use in a multiprogramming and/or multiprocessing environment.

The specific nature of the invention as well as other objects, advantages, features and uses thereof will become apparent from the following detailed description taken in conjunction with the accompanying drawings.

Brief description of the drawings.

Fig. 1 is a schematic and electrical diagram illustrating a preferred embodiment of the invention.

Fig. 2 is a schematic and electrical diagram illustrating details of the Fig. 1 embodiment.

Fig. 3 is a series of tables illustrating the operation of the multiplexers in Fig. 2.

Detailed description of the invention

Like numerals refer to like elements throughout the drawings.

Referring to Fig. 1, illustrated therein is a preferred embodiment of register allocation apparatus in accordance with the invention. As shown, an allocation register 10 is provided whose states indicate the free and assigned states of a plurality of assignable registers. For the purposes of this description and by way of example, it will be assumed that there are sixteen registers R1 to R16 available for assignment. Accordingly, the allocation register 10 will be assumed to contain sixteen bit storage elements r_1—r_{16} respectively corresponding to the assignable registers R1—R16, wherein a "0" value of a bit storage element is used to indicate that its corresponding register is unavailable for assignment, while a "1" value indicates that the corresponding register is free and thus available for assignment. It will further be assumed by way of example that, at a particular point in time, the sixteen bit elements r_1—r_{16} of the allocation register 10 have the respective values 0101010001101010 shown in Fig. 1. Thus, register 10 in Fig. 1 indicates that the seven registers R2, R4, R6, R10, R11, R13 and R15 are free registers.

As indicated in Fig. 1, the first eight bit storage elements r_1—r_8 of the allocation register 10 are applied as an address to a first memory 15 and the second eight bit storage elements r_9—r_{16} are applied as an address to a second memory 20. Each of these memories 15 and 20 may typically be a PROM (programmable read only memory). Generally, the construction and operation of the preferred embodiment of Fig. 1 is such that appropriate portions of the selected memory words read out from memories 15 and 20 (in response to the respective addresses provided by the allocation register 10) are applied to a comparator 25 for determining whether a sufficient number of free registers are available for a newly activated task, and are also applied to a plurality of multiplexers 30 for identifying a particular number of free registers available for assignment to a newly activated task based on the current state of the elements r_1—r_{16} of the allocation register 10. These free register identification and a corresponding task identifacation number are stored in a register mapper 40 so that, when the register mapper 40 is accessed during task execution, these register identifications are read out

and applied to a register file 45 for accessing the identified registers.

The construction and operation of Fig. 1 will now be considered in more detail with reference to Fig. 2. For this purpose, and by way of example, it will be assumed that each task requires a maximum of five free registers. Accordingly, multiplexers 30 in Fig. 1 are shown in Fig. 2 as comprising the five multiplexers 31—35 whose outputs M_1—M_5 are binary numbers identifying five particular free registers available for assignment to a newly activated task based on the current states of the bit storage elements of the allocation register 10. For the illustrated embodiment of Fig. 2, it is assumed that these five free registers identified by the multiplexer outputs M_1—M_5 are the five lowest numbered free registers currently available, which, in conformance with the states of the allocation register 10, are registers R2, R4, R6, R10 and R11.

In order to permit the mapping of memories 15 and 20 to be readily understood, Fig. 2 illustrates examples of the particular selected memory words W—A and W—B read out from memories 15 and 20, respectively, in response to the illustrated states of their corresponding portions of the allocation register 10 shown in Fig. 1. It will be understood that, for greater clarity, decimal numbers are used in Fig. 2 to indicate the contents of the various memory work portions; however, these decimal numbers are preferably stored in binary form in memories 15 and 20. It will also be understood that the selected memory word W—A from memory 15 provides data relative to registers R1—R8 (since memory 15 is addressed by elements r_1—r_8 of register 10), while the memory word W—B from memory 20 provides data relative to registers R9—R16 (since memory 20 is addressed by elements r_9—r_{16} of register 10). Thus, proceeding from left to right, the left-most portion of each memory word contins a number (designated SA for memory word W—A and SB for memory word W—B) indicating the total number of free registers in accordance with the states of the respective elements of the allocation register 10 in Fig. 1. The next portion of each memory word (designated 1A, 2A, 3A, 4A, 5A for memory word W—A and 1B, 2B, 3B, 4B, 5B for memory word W—B) identifies (also in accordance with its respective elements of register 10) up to five free registers beginning with the lowest number free register; an "X" indicates that no additional free registers are available besides those indicated any may typically have a "don't care" value such as "0" (since there is no "0" register).

Thus, for memory word W—A in Fig. 2, SA properly indicates a total of three free registers for W—A, and SB properly indicates a total of four free registers for W—B. Also, 1A, 2A and 3A of memory word W—A respectively identify the three free registers 2, 4 and 6 indicated by elements r_1—r_8 of register 10, while 4A and 5A are properly indicated as "X" (don't care) values (since elements r_1—r_8 indicate no other free registers). In a similar manner, 1B, 2B, 3B, 4B of memory word W—B respectively identify the four free registers 10, 11, 13 and 15 indicated by elements r_9—r_{16} of register 10, while 5B indicates a "don't care" value (since elements r_9—r_{16} indicate no other free registers).

It will be noted in Fig. 2 that memory word W—A additionally includes portions designated as m_1, m_2, m_3, m_4 and m_5. These portions could alternatively be included with memory word W—B or they could be split up between the two memory words. As indicated in Fig. 2, these m_1, m_2, m_3, m_4, m_5 portions are respectively applied as selection signals to multiplexers M1, M2, M3, M4 and M5, and different pluralities of portions 1A to 5A and 1B to 5B of memory words W—A and W—B are respectively applied as register identification input signals to each of multiplexers M1—M5. As is to be expected, the size of each of the multiplexers M1—M5 and the number of bits required for each of m_1—m_5 are dependent on the number of 1A to 5A and 1B to 5B input applied to each multiplexer.

The choice of the values of m_1—m_5 and the particular pluralities of portions 1A to 5A and 1B to 5B to be applied to each of multiplexers M1—M5 in Fig. 2 is based on obtaining, at the multiplexer outputs, identifications of a particular group of free registers for assignment to each newly activated task. In the preferred embodiment, this particular group of free registers is chosen as the five lowest numbered free registers which, for the exemplary states of the allocation register 10 illustrated in Fig. 1, are registers R2, R4, R6, R10 and R11 as indicated at the multiplexer outputs in Fig. 2. The tables of Fig. 2 set forth the operation of the multiplexers M1—M5 in response to the respective m_1—m_5 and 1A to 5A and 1B to 5B signals applied thereto (as shown in Fig. 2), whereby the five lowest numbered free registers are identified at the multiplexer outputs.

The tables of Fig. 3 will now be considered in more detail with specific reference to the exemplary values of the memory words W—A and W—B illustrated in Fig. 2.

It will be understood from Figs. 2 and 3 that multiplexer M1 has only the two inputs 1A and 1B from memory words W—A and W—B applied thereto so that its selection input m_1 need only be a single bit. Since 1A of memory word W—A contains a "2" identifying R2 as the lowest number free register, the value of m_1 for word W—A is chosen as a "0" to cause the contents of 1A (which identifies register R2 as a free register to be selected as the output of multiplexer M1. In this regard, it is to be noted that the respective m_1, m_2, m_3, m_4, m_5, inputs for the multiplexers M1—M5 in the preferred embodiment are chosen so that each muliplexer selects the lowest numbered input of the particular plurality of 1A—5A and 1B—5B inputs applied thereto which identifies a free register, with an "A" input being selected ahead of a "B" input.

As indicated in Fig. 2 multiplexer M2 has the

three inputs 2A, 1B and 2B of memory word W—A and W—B applied thereto so that m_2 requires two bits for selecting among 2A, 1B and 2B, as illustrated in the multiplexer M2 table in Fig. 3. Since 2A of memory word W—A contains a"4" identifying R4 as a free register, m_2 for word W—A is chosen as "00" to cause the content of 2A (which identifies register R4 as a free register) to be selected as the output of multiplexer M2.

Multiplexer M3 in Fig. 2 has the four inputs 3A, 1B, 2B, 3B from memory words W—A and W—B applied thereto which, like m_2, requires a two bit m_3 input for selection as illustrated in Fig. 3. Since 3A of memory word W—A contains a "6" identifying R6 as a free register, m_3 for word W—A is chosen as "00" to cause the contents of 3A (which identifies register R6 as a free register) to be selected as the output of multiplexer M3.

Multiplexer M4 in Fig. 2 has the five inputs 4A, 1B, 2B, 3B, 4B from memory words W—A and W—B applied thereto which requres a three bit m_4 input for selection as illustrated in Fig. 3. The first free register identified by the inputs applied to M4 is indicated by 1B which contains a"10" identifying register R10 as a free register. Thus, in accordance with Fig. 3, m_4 is chosen as "001" to cause the contents of 1B to be selected as the output of multiplexer M4.

The remaining multiplexer M5 in Fig. 2 has the six inputs 5A, 1B, 2B, 3B, 4B, 5B from memory words W—A and W—B applied thereto which, like m_4, requires a three bit m_5 input for selection as illustrated in Fig. 3. The first free register identified by the inputs applied to M5 is indicated by 2B which contains an "11" identifying register R11 as a free register. Thus, in accordance with Fig. 3, m_5 is chosen as 010 (which is "2" in decimal) to cause the contents of 2B to be selected as the output of multiplexer M5.

Referring back to Fig. 1, it will be seen that the free register identifications provided at the output of the multiplexers 30 are applied to an update circuit 50 along with the number of free registers required by the task. The update circuit 50 responds to these inputs by providing an output to the allocation register 10 which updates the values of the storage elements r_1—r_{16} accordingly.

Having described how selection of the five lowest numbered free registers is accomplished in the preferred embodiment illustrated in Figs. 1—3, it will next be considered how the situation is handled by the preferred embodiment when there are insufficient free registers available for assignment to a newly activated task.

It will be remembered that the SA and SB portions of memory words W—A and W—B contain the total number of free registers indicated by their respective portions of the allocation register 10 in Fig. 1. Accordingly, these SA and SB values are applied to the comparator 25 which also receives an input indicating the number of free registers required by a newly initiated task. The comparator 25 compares the sum of SA and SB with the number of free registers required by the task. If insufficient free registers are available, the comparator 25 produces a HOLD signal which is used to cause the task to wait until sufficient free registers are available.

Claims

1. For use in a data processing system, resource allocation apparatus comprising:

storage means indicating the free and assigned states of a plurality of resources, said storage means including a plurality of portions, each portion indicating the free and assigned states of a particular predetermined plurality of said resources;

a plurality of individually addressable memories, each memory being addressed by a respective one of said portions and being operative in response thereto for providing a corresponding memory output including free resource identifying signals which identify at least a predetermined plurality of the free resources indicated by the applied address, the memory outputs from said memories also including a plurality of selection signals; and

a plurality of selection means to which said memory outputs are applied, each selection means receiving particular ones of said resource identifying signals and said selection signals and being operative in response thereto so that the outputs of said selection means identify a particular predetermined plurality of the free resources indicated by said storage means.

2. The invention in accordance with claim 1, wherein said selection means comprises a plurality of multiplexers, one for each resource to be identified, wherein each multiplexer receives as a multiplexer input a different predetermined plurality of said free resource identifying signals provided by said memory outputs, and wherein each multiplexer receives as a seection input a respective one or more of said selection signals provided by said memory outputs.

3. The invention in accordance with claim 2, wherein said multiplexers successively receive a greater number of said resource identifying signals.

4. The invention in accordance with claim 1, wherein each of said memories is a programmable read only memory.

5. The invention in accordance with claim 1, 2, 3 or 4, including updating means responsive to the outputs of said selection means for updating said storage means.

6. The invention in accordance with claim 1, 2 or 3, wherein each memory stores a plurality of individually addressable memory words, one of which is selected by the applied address for providing the memory output of the memory, wherein each memory word contains resource identifying data identifying at least a predetermined plurality of the free resources indicated by the applied memory address, said resource identifying data corresponding to the resource identifying signals in the memory output, and wherein

the memory words of at least one memory includes a plurality of selection data items, one item for each selection means, said selection data items corresponding to said selection signals in the memory output.

7. The invention in accordance with claim 6, wherein said selection data items are chosen in conjunction with the choice of the predetermined plurality of resource identifying signals applied to each selection means so that a predetermined ordered group of free resources are identified at the outputs of said selection means.

8. The invention in accordance with claim 7, wherein said resources are designatable in a particular numerical order, and wherein the choice of said selection data items and the choice of the predetermined plurality of resource identifying signals applied to each selection means are such that the lowest numbered free resources are identified at the outputs of said selection means.

9. The invention in accordance with claim 1, 2 or 3 wherein said system operates by performing a plurality of tasks, wherein each task requires the assignment of one or more free rsources thereto, and wherein resource mapping means are provided for storing the outputs of said selection means and a corresponding task identification.

10. The invention in accordance with claim 1, 2 or 3 wherein each memory output also includes signals representing the number of free resources indicated by its respective portion of said storage means, and wherein comparison means are provided responsive to these signals representing the number of free resources for providing a hold indication when there are insufficient free resources available for a task.

11. The invention in accordance with anyone of claims 1 to 10, wherein said plurality of resources are a plurality of registers.

Patentansprüche

1. Betriebsmittel-Zuordnungsanordnung für ein Datenverarbeitungssystem mit:

einer Speichereinrichtung, die die freien und zugewiesenen Zustände mehrerer Betriebsmittel anzeigt und mehrere Abschnitte enthält, von denen jeder den freien und zugewiesenen Zustand einer besonderen, vorbestimmten Vielzahl der Betriebsmittel angibt; mehreren individuell adressierbaren Speichern, von denen jeder von einem entsprechenden der Abschnitte adressiert wird und auf eine Adressierung ein entsprechendes Speicherausgangssignal abgibt, das Freie-Betriebsmittel-Identifizierungssignale enthält, die mindestens eine vorbestimmte Anzahl der freien Betriebsmittel identifiziert, die durch die verwendete Adresse angegeben sind, wobei die Speicherausgangssignale der Speicher auch meherer Auswahlsignale enthalten; und mehrere Auswahleinrichtungen, denen die Speicherausgangssignale zugeführt werden, wobei jede Auswahleinrichtung spezielle Betriebsmittel-Identifizierungssignale und die Auswahlsignale empfängt und auf deren Empfang so reagiert, daß die Ausgänge der Auswahleinrichtungen eine besondere, vorbestimmte Anzahl der freien Betriebsmittel identifizieren, die durch die Speichereinrichtung angegeben werden.

2. Anordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Auswahleinrichtung mehrere Multiplixer enthält, von denen einer für jedes zu identifizierende Betriebsmittel vorgesehen ist, wobei jeder Multiplexer als Multiplexer-Eingangssignal eine verschiedene, vorbestimmte Anzahl der Freie-Betriebsmittel-Identifizierungssignal empfängt, die von den Speicherausgängen abgegeben werden, und wobei jeder Multiplexer als Auswahleingang eins bzw. mehrere der Auswahlsignale empfängt, die von den Speicherausgängen abgegeben werden.

3. Anordnung nach Anspruch 2, dadurch gekennzeichnet, daß die Multiplexer nacheinander eine größere Anzahl der Betriebsmittel-Identifizierungssignale empfangen.

4. Anordnung nach Anspruch 1, dadurch gekennzeichnet, daß jeder der Speicher ein programmierbarer Festspeicher (PROM) ist.

5. Anordnung nach Anspruch 1, 2, 3 oder 4, gekennzeichnet durch eine Fortschreibungseinrichtung, die auf die Ausgangssignale der Auswahleinrichtung die Speichereinrichtung auf den neuesten Stand bringt.

6. Vorrichtung nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß jeder Speicher mehrere individuelle adressierbare Speicherworte speichert, von denen jedes durch die verwendete Adresse zur Abgabe des Speicherausgangssignals des Speichers verwendet wird, wobei jedes Speicherwort Betriebsmittel-Identifizierungsdaten enthält, die mindestens eine vorbestimmte Anzahl freier Betreibsmittel identifizeirt, die durch die verwendete Speicheradresse angezeigt sind, wobei die Betriebsmittel-Identifizierungsdaten, den Betriebs mittelsignalen im Speicherausgang entsprechen, und daß die Speicherworte mindestens eines Speichers mehrere Auswahldatengrößen enthalten, wobei eine größe für jede Auswahleinrichtung vorgesehen ist, und wobei die Auswahldatengrößen den Auswahlsignalen im Speicherausgang entsprechen.

7. Anordnung nach Anspruch 6, dadurch gekennzeichnet, daß die Auswahldatengrößen in Verbindung mit der Wahl der vorbestimmten Anzahl Betriebsmittel-Identifizierungsignale gewählt sind, die an jede Auswahleinrichtung gelegt werden, so daß eine vorbestimmte, geordnete Gruppe freier Betriebsmittel an den Ausgängen der Auswahleinrichtung identifiziert wird.

8. Anordnung nach Anspruch 7, dadurch gekennzeichnet, daß die Betriebsmittel in einer bestimmten numerischen Reihenfolge bestimmbar sind. und daß die Wahl der Auswahldatengrößen und die Wahl der vorbestimmten Anzahl Betriebsmittel-Identifizierungssignale, die an jede Auswahleinrichtung gelegt werden, so sind, daß die niedrigst bezifferten freien Betriebsmittel an den Ausgängen der Auswahleinrichtung identifiziert werden.

9. Anordnung nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß das System mehrere Aufgaben durchführt, wobei jede Aufgabe die Zuordnung einer oder mehrerer freier Betriebsmittel dafür erfordert und daß Betriebsmittelmappingeinrichtungen zum Speichern der Ausgangssignale der Auswahleinrichtungen und einer entsprechenden Aufgabenidentifikation vorgesehen sind.

10. Anordnung nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß jeder Speicherausgang auch Signale enthält, die die Anzahle freier Betriebsmittel, die von ihrem entsprechenden Abschnitt der Speichereinrichtung angezeigt werden, repräsentieren, und daß Vergleichseinrichtungen vorgesehen sind, die auf den Empfang dieser die Anzahl freier Betriebsmittel repräsentierenden Signale eine Halteanzeige abgeben, wenn nicht genügend freie Betriebsmittel für eine Aufgabe verfügbar sind.

11. Anordnung nach einem der vorstehenden Ansprüche 1 bis 10, dadurch gekennzeichnet, daß die mehreren Betriebsmittel mehrere Register sind.

Revendications

1. Appareil d'affectation de ressources applicable à un système de traitement de données caractérisé en ce qu'il comporte:

un moyen de stockage indiquant les états libres et attribués d'un ensemble de ressources, ce moyen de stockage comprenant un ensemble de parties, chaque partie indiquant l'état libre et l'état attribué d'un ensemble prédéterminé, paricular de ressources;

un emsemble de mémoires adressables séparément, chaque mémoire étant adressée par une partie respective et étant mise en oeuvre en réponse pour fournir un signal de sortie de mémoire correspondant comprenant des signaux d'identification de ressources libres que identifient au moins un ensemble prédéterminé de ressources libres indiquées par l'adresse fournie, les signaux de sortie des mémoires comportant également un ensemble de signaux de sélection et,

un ensemble de moyens de sélection auxquels sont appliqués les signaux de sortie de mémoire, chaque moyen de sélection recevant un des signaux d'identification de ressources et ces signaux de sélection pouvant être mis en oeuvre en réponse à cet envoi de façon que les signaux de sortie du moyen de sélection identifient un ensemble prédéterminé particulier de ressources libres indiquées par le moyen de stockage.

2. Appareil selon la revendication 1, caractérisé en ce que le moyen de sélection comprend un ensemble de multiplexeurs, un multiplexeur pour chaque ressource à identifier et chaque multiplexeur reçoit comme signal d'entrée de multiplexeur un ensemble prédéterminé, différent de signaux d'identification de ressources libres fournis par les sorties de mémoire et chaque multiplexeur reçoit comme entrées de sélection un ou plusieurs signaux de sélection respectifs fournis par les signaux de sortie de mémoire.

3. Appareil selon la revendication 2, caractérisé en ce que les multiplexeurs reçoivent successivement un nombre plus grand de signaux d'identification de ressources.

4. Appareil selon la revendication 1, caractérisé en ce que chacune des mémoires est une memoire morte programmable.

5. Appareil selon les revendications 1, 2, 3 ou 4, caractérisé en ce qu'il comporte un moyen de mise à jour répondant aux signaux de sortie du moyen de sélection pour mettre à four le moyen de stockage.

6. Appareil selon les revendication 1, 2 ou 3, caractérisé en ce que chaque mémoire enregistre un ensemble de mots de mémoire adressables separement, l'un des mots éant susceptibles d'être choisi par l'adresse qui lui est appliquée pour fournie le signal de sortie de mémoire, chaque mot de memoire contenant une donnée d'identification de ressources identifiant au moins un ensemble prédéterminé de ressources libres indiquées par l'adresse de mémoire, les données d'identification de ressources correspondant aux signaux d'identification de ressources dans la sortie de mémoire et les mots de mémoire d'au moins une mémoire comprenant un ensemble d'élément de données de sélection, un élément pour chaque moyen de sélection, ces éléments de données de sélection correspondant aux signaux de sélection dans la sortie de mémoire.

7. Appareil selon la revendication 6, caractérisé en ce que les éléments de données de sélection sont choisis en liaison avec le choix de l'ensemble prédéterminé de signaux d'identification de ressources appliquées à chaque moyen de sélection de façon à identifier un groupe ordonné prédéterminé de ressources libres sur les sorties des moyens de sélection.

8. Appareil selon la revendication 9, caractérisé en ce que les ressources peuvent être désignées à nouveau dans un ordre numérique particulier et le choix des éléments de données de sélection ainsi que le choix de l'ensemble prédéterminé de signaux d'identification de ressources apliqués à chaque moyen de sélection sont tels que les ressources libres de numéro le plus bas soient identifiées à la sortie des moyens de sélection.

9. Appareil selon les revendications 1, 2, 3, caractérisé en ce que le système fonctionne en exécutant un ensemble de travaux, chaque travail nécessitant l'affectation d'une ou plusieurs ressources libres à ce travail et des moyens formant la carte des ressources étant prévus pour enregistrer les signaux de sortie du moyen de sélection et une identification correspondante de taches.

10. Appareil selon les revendications 1, 2 et 3, caractérisé en ce que chaque signal de sortie de mémoire contient également des signaux représentant le nombre de ressources libres indiquées par ses parties respectives du moyen de stockage, les moyens de comparaison étant prévus pour être mis en oeuvre par ces signaux représentant le nombre de ressources libres pour fournir une

indication de maintien lorsque le nombre de ressources libres disponibles pour un travil n'est pas suffisant.

11. Appariel selon l'une quelconque des revendications 1 à 10, caractérisé en ce que l'ensemble des ressources est un ensemble de registres.

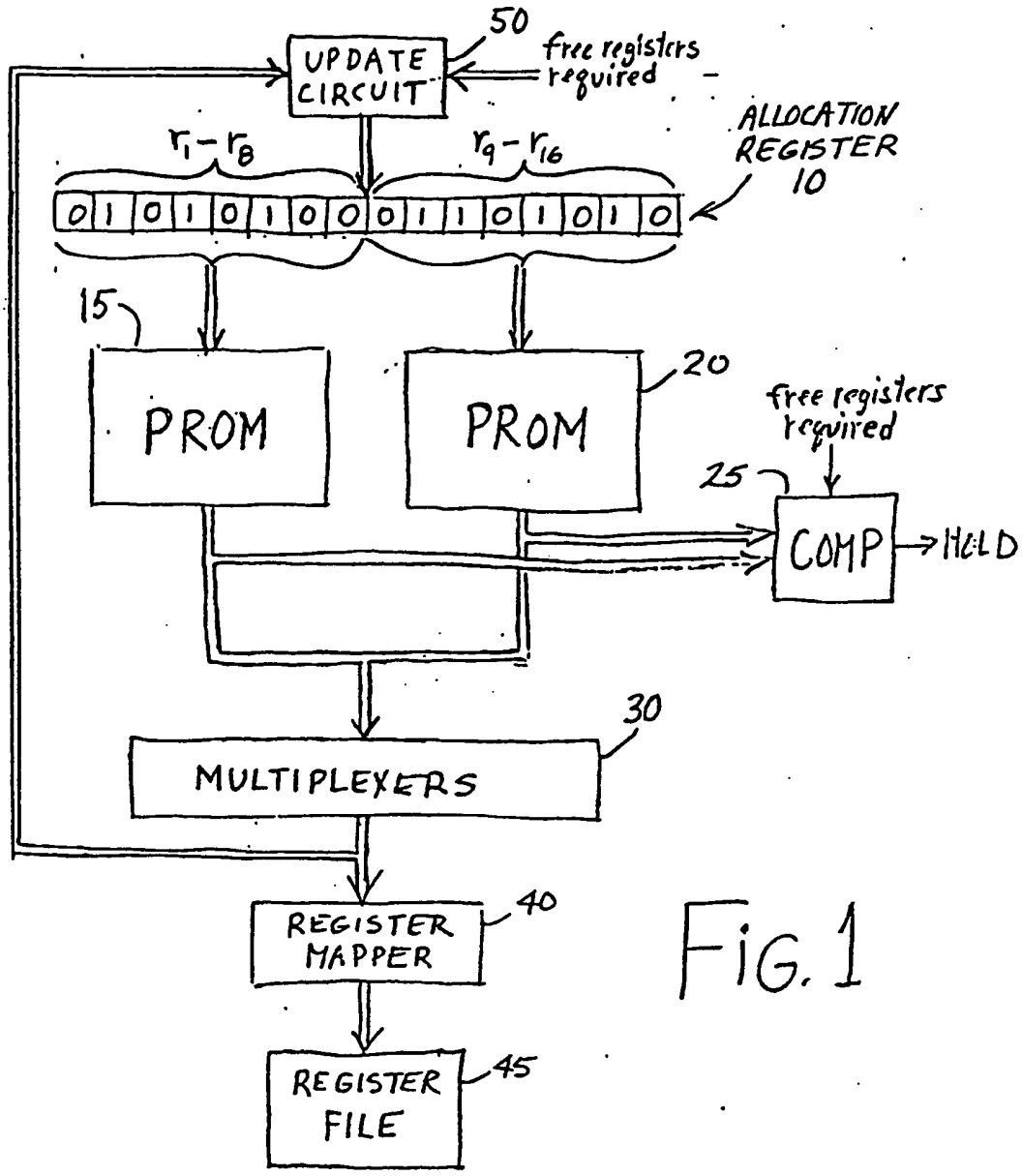
50
UPDATE CIRCUIT
free registers required
ALLOCATION REGISTER 10
$r_1 - r_8$
$r_9 - r_{16}$
0 1 0 1 0 1 0 0 0 1 1 0 1 0 1 0
15
PROM
PROM
20
free registers required
25
COMP
HOLD
30
MULTIPLEXERS
40
REGISTER MAPPER
45
REGISTER FILE

FIG. 1

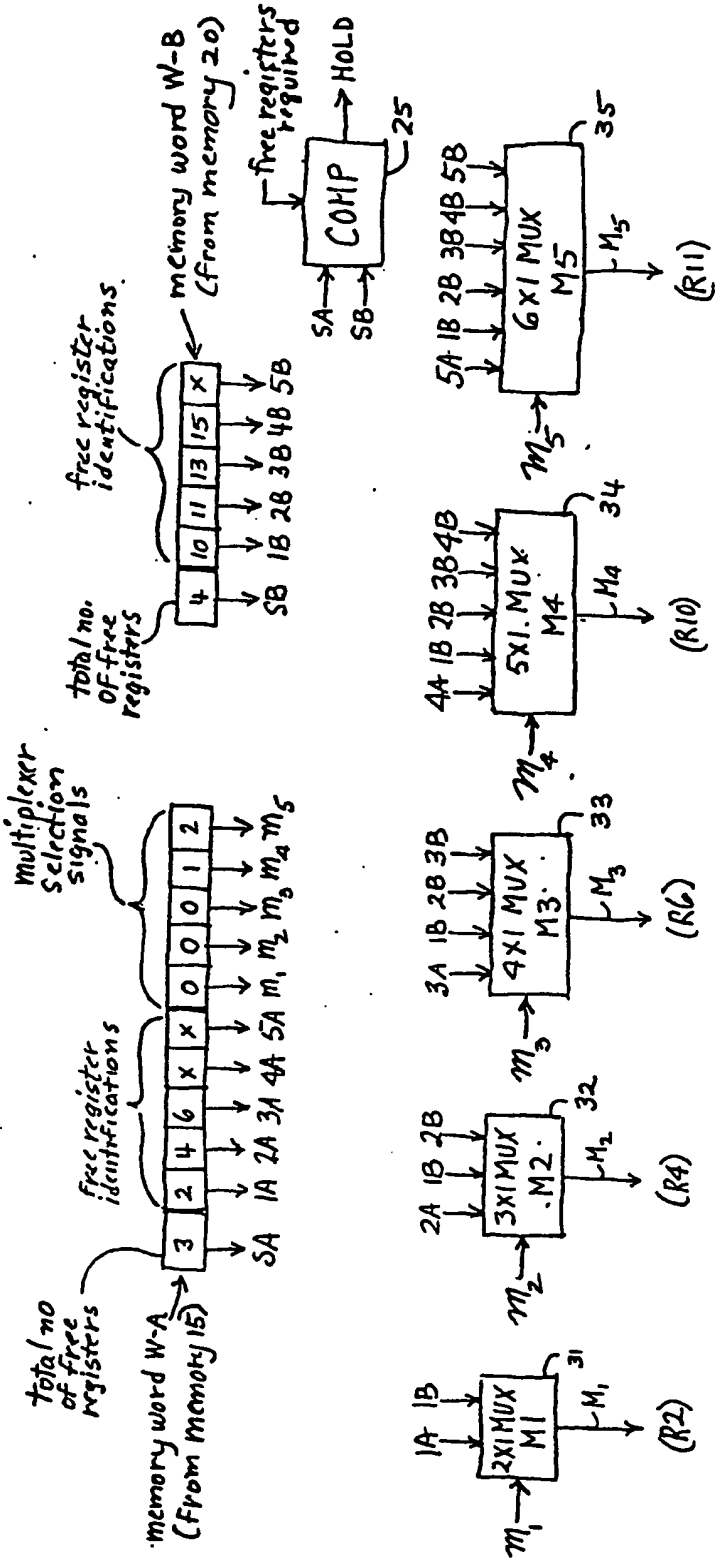
total no of free registers
memory word W-A (From memory 15)
free register identifications
multiplexer selection signals
3 2 4 6 X X 0 0 0 2
5A 1A 2A 3A 4A 5A m1 m2 m3 m4 m5
total no. OF free registers
memory word W-B (From memory 20)
free register identifications
4 10 11 13 15 X
5B 1B 2B 3B 4B 5B
free registers required
COMP
SA
SB
HOLD
25
1A 1B
2X1 MUX M1
m1
31
M1
(R2)
2A 1B 2B
3X1 MUX M2
m2
32
M2
(R4)
3A 1B 2B 3B
4X1 MUX M3
m3
33
M3
(R6)
4A 1B 2B 3B 4B
5X1 MUX M4
m4
34
M4
(R10)
5A 1B 2B 3B 4B 5B
6X1 MUX M5
m5
35
M5
(R11)

Fig. 2

MULTIPLEXER M1 INPUTS: 1A, 1B		MULTIPLEXER M2 INPUTS: 2A, 1B, 2B		MULTIPLEXER M3 INPUTS: 3A, 1B, 2B, 3B		MULTIPLEXER M4 INPUTS: 4A, 1B, 2B, 3B, 4B		MULTIPLEXER M5 INPUTS: 5A, 1B, 2B, 3B, 4B, 5B	
m_1	M_1	m_2	M_2	m_3	M_3	m_4	M_4	m_5	M_5
0	1A	00	2A	00	3A	000	4A	000	5A
1	1B	01	1B	01	1B	001	1B	001	1B
–	–	10	2B	10	2B	010	2B	010	2B
–	–	–	–	11	3B	011	3B	011	3B
–	–	–	–	–	–	100	4B	100	4B
–	–	–	–	–	–	–	–	101	5B

Fig. 3

0 075 633